SPECIFICATIONS

GENERAL

ADC Type: Gated current integrating Wilkinson, 13-bit resolution.
Signal Inputs: 64 input channels. Can be configured as 50 Ω single-ended or 100 Ω quasi-differential. Inputs are diode protected.
Signal Input Connector: Four 34-pin front-panel headers.
Gate Input: Differential ECL input either front-panel, or FASTBUS TR1 and TR2, 50 - 500 nsec.
Common Mode Rejection Ratio: > 50 dB for ±200 mV DC to 1 kHz[1].
Conversion In Progress (CIP) Output: Front-panel differential ECL, indicating that the unit is not yet ready for another gate input.
Fast Clear: Differential ECL front-panel or single-ended TR0 back panel signal. If the clear is applied within 7 μsec after the trailing edge of the gate then a gate may be applied 1 μsec later with less than a 2 count pedestal shift. If the clear is applied between 7 μsec after the trailing edge of the gate and the end of the Fast Clear window a gate may be applied after 400 nsec with less than a 1 count pedestal shift.
Pedestal: 200 - 800 counts.
Full Scale: 8192 counts above the pedestal.
Sensitivity: 100 fC/count.
Integral Linearity: ±6 counts maximum.
Differential Non-Linearity: ±15% from 10 - 100% full scale. (±7% typical)
Operating Region: +10 mV to -1.5 V for specified linearity, (+0.2 mA to -30 mA into 50 Ω)[1].
Noise: 0.7 count R.M.S. typical, 1 count maximum, tested with constant conversion rate and disconnected inputs, without readout during conversion.
Interchannel Isolation: 75 dB typical, 66 dB minimum.
Temperature Coefficient: ±(0.05% of reading + 1 count)/C, inputs unconnected or capacitively-coupled[1].
Long Term Stability: ±(0.25% of reading + 1 count)/week[1].
Conversion Time: 12 μsec for all 64 channels. May be configured as 12 bit 100 fC resolution unit with conversion time of 9 μsec.
Multiple Event Buffer: Digital memory for 64 events.
Data Compaction: Only the contents of channels greater than their programmable threshold will be stored.
Fast Clear Window: If the fast clear is guaranteed to always occur before the end of conversion then the Fast Clear Window (FCW) can be set equal to the conversion time. In this case there is NO conversion time penalty for the fast clear window. If longer fast clear windows are required they can be programmed up to 32 μsec in 2 μsec steps. In this case the end of conversion will be extended to the end of the FCW.
Pedestal Gate Width Dependence: < 25 fC/nsec.
Self Test Feature: Needs an external DC voltage and a Gate signal (e.g., from Model 1810 CAT); voltage range is 0 to 10 V.
Power Requirements: +15 V at 0.7 A; +5 V at 5 A; -2 V at 2 A; -5.2 V at 6 A; -15 V at 0.1 A.
Packaging: Single-width FASTBUS module (ANSI/IEEE 960-1989).

FASTBUS CONTROL

Addressing Modes: Geographic, Logical, and Broadcast (all classes). Implemented Registers, FIFO.
Implemented Addressing Modes: Logical (16 bits), Geographical, Broadcast.
AS-AK Handshake Time: 125 nsec typical, 150 nsec maximum.
DS-DK Handshake Time: 65 nsec typical, 75 nsec maximum.
Module Identification Code: $104F_h$.

CSR 0_h	Module ID and control status.
CSR 1_h	FCW settings and gate and clear routing.
CSR 3_h	Logical address.
CSR 5_h	Word count for block transfers (automatically loaded by LOAD NEXT EVENT command (CSR0 bit 8)).
CSR 7_h	Broadcast class.
CSR 10_h	Read\writeable pointers to circular buffer automatically advanced by incoming events and LOAD NEXT EVENT command.
CSR $C0000000_h$	Sparsification thresholds one per
CSR $C000003F_h$	channel.

Slave Status Responses to Data Cycles:

SS	*Significance*
0	Valid Action
2	End of Data
7	Error. Invalid Secondary Address loaded into internal address register.

[1] *Sample Tested.*

IMPLEMENTED BROADCAST FUNCTIONS

Code	Significance	Comments
01_{h*}	General Broadcast Select	The 1881M modules are selected and respond to subsequent data cycles.
$X5_h$	Class N Broadcast	The 1881M with class bit X set are selected and respond to subsequent data cycles.
09_h	Sparse Data Scan	1881M modules containing at least one event assert the T pin on the following read data cycle.
$0D_h$	All Device Scan	All 1881M modules assert their T pin on the following read data cycle.
$9D_h$	ADC Sparse Data Scan	Unique Sparse Data Scan for 1880 Series modules only. Follows standard Sparse Data Scan (see above).
CD_h	ADC Data Scan	Second level sparse data scan for 1881/1881M modules. ADCs with at least one data word above threshold for the current event waiting to be read out will assert T pin.

* An h subscript indicates hexadecimal (base 16).